ABSTRACT OF THE DISCLOSURE

A system can be realized by using a single frame memory, that is costly, to allow data write and data read operations continuously without suspending the video signal input. Such a memory controller comprises a serial/parallel converter section for converting serial input data into parallel data, an FIFO memory section for temporarily storing converted data, a memory section connected to the FIFO memory section to store data for a frame and a second FIFO memory section for temporarily storing the data read out from the frame memory section. The data bit width of said memory section is made equal to n times of the bit width of said input data so that data for a number of frames up to as many as (n-2) times of the number of input pixels can be read out of said memory section for said input data while the frequency of accessing said memory section can be reduced to a half or less than a half of the video signal input frequency.